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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/770,478	01/29/2001	James R. Del Signore II	AXI-144	6823

7590 05/31/2002

George R.McGuire Hancock & Eatabrook LLP
1500 Mony Tower I
Po Box 4976
Syracuse, NY 13221-1976

EXAMINER	
TRA, ANH QUAN	
ART UNIT	PAPER NUMBER
2816	9

DATE MAILED: 05/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/770,478	DEL SIGNORE II ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-8 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the amendment filed 04/16/2002. A new ground of rejection is introduced in view of applicant's necessitated amendment.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Kinoshita et al. (USP 6150800) (newly cited).

As to claims 1, Kinoshita et al. discloses in figure 11 an inrush circuit comprising: means (10) for providing a voltage ramp; means (output node 4) defining an output voltage (OUT); an operational amplifier circuit (2 except 10) having a reference input, the operational amplifier circuit receiving the voltage ramp at the reference input and comparing a divided sample (by voltage divider 51, 52) of the output voltage with the voltage ramp, the operational amplifier operating in a linear mode, whereby the output voltage approximate a multiple of voltage ramp; transistor means (1) electronically connected to the operational amplifier circuit, the transistor means operating in linear mode during capacitor charging, subsequently reaching a full-O state; and energy storage load means (3) connected to the transistor means for receiving a full power supply after the transistor means reaches its full-ON state.

As to claim 6, it is inherent for field effect transistor is operative initially in an OFF state, and subsequently becomes operative in a full-ON state.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita et al. (USP 6150800).

As to claim 2, Kinoshita et al.'s figure 11 shows all limitations of the claim except for the transistor is a power FET. However, it is well known in the art that power FET is for operating in high power condition. Therefore, it would have been obvious to one having ordinary skill in the art to make transistor 1 or all transistors as a power transistor for the purpose of operating in a high power condition.

As to claim 3, it is seen as an obvious design choice for selecting gain value of the amplifier to be two (2) dependent upon particular environment of use to ensure optimum performance.

As to claim 4. it is seen as an intended use for selecting the output node to be a point-of-sale printer.

As to claim 17, figure 11 shows all limitations of the claim except for a delay means connected to means for providing a voltage ramp. However, it is well known in the art that a buffer circuit is for delaying signal of buffering signal. Therefore, it would have been obvious to

one having ordinary skill in the art to add a buffer circuit to buffer the control signal that controlling switch circuit (18) in circuit 10 for the purpose of buffering or delaying the control signal.

As to claim 18, it is seen as an obvious design choice for selecting the delay time of the delay means to be approximately 50 ms dependent upon particular environment of use to ensure optimum performance.

As to claim 19, it is seen as an obvious design experiment for selecting the energy storage means to be a bulk capacitor dependent upon particular environment of use to ensure optimum performance.

5. Claims 7 and 8, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita (USP 6150800) in view of (USP 5818212) and Kajimoto (USP 5557193).

Kinoshita et al.'s figure 1 shows all limitations of the claim except for a capacitive means electronically connected to the field effect transistor for ensuring that the field effect transistor is initially operative in the OFF state. However, Kajimoto's figure 1 shows a circuit having capacitor 12 for ensuring transistor (MOUT) is initially in the OFF state and providing a good transient characteristic for the circuit. Therefore, it would have been obvious to one having ordinary skill in the art to add a capacitor coupled between the output of the amplifier and output of Kinoshita 's circuit for the purpose of ensuring the transistor 12 initially in the OFF state and providing a good transient characteristic for the circuit.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
May 20, 2002

Terry D. Cunningham
Primary Examiner